CLAIMS

What is claimed is:

1. A resetable memory, comprising:

a memory without reset capability having a data output coupled to a first input of a first multiplexer, a second input of said first multiplexer having a reset value input, a channel select for said first multiplexer coupled to a resetable storage cell output that indicates whether a storage cell within said memory without reset capability has been written to after a reset or has not been written to after a reset.

2. The resetable memory of claim 1 wherein said resetable storage cell is a storage cell within a memory unit having reset capability.

3. The resetable memory of claim 1 wherein said resetable storage cell is a register.

4. The resetable memory of claim 3 further comprising a second multiplexer having an output coupled to an input of said register, a first input of said second multiplexer having a value opposite said register's reset value, a second input of said second multiplexer coupled to said register's output, said second multiplexer having a channel select that is indicative of whether or not said storage cell is being written to, said first input of said second multiplexer enabled if said cell is being written to.

5. The apparatus of claim 4 wherein said channel select of said second multiplexer is an output of a logic gate that receives a write enable signal and a signal that indicates whether said cell is being addressed.

6. The apparatus of claim 5 wherein said logic gate is an AND gate.

7. The apparatus of claim 3 wherein said channel select for said first multiplexer is coupled to said register through a second multiplexer that receives said register output and a second register output that indicates whether a second cell within said memory without reset capability has been written to after a reset or has not been written to after a reset, said second multiplexer output coupled to said first multiplexer channel select.

8. The apparatus of claim 7 wherein said second multiplexer channel select is an address into said memory without reset capability.

9. The apparatus of claim 1 wherein said reset value input is coupled to an output of a reset value function circuit, said reset value function circuit having an input coupled to an address input to said memory unit with reset.

10. The resetable memory of claim 1 further comprising a circuit that uses said resetable memory to implement a random access memory (RAM).

11. The resetable memory of claim 1 further comprising a circuit that uses said resetable memory to implement a FIFO.

12. The resetable memory of claim 1 further comprising a circuit that uses said resetable memory to implement a shift register.

13. The resetable memory of claim 1 further comprising a circuit that uses said resetable memory to implement a content addressable memory (CAM).

14. A method comprising:

presenting a reset value as a read value from a storage cell of a memory unit without reset if said storage cell has not been written to after a reset has been applied, said reset value not an actual output value of said memory unit without reset; and

presenting said actual output value of said memory unit without reset as said read value if said storage cell has been written to after said reset has been applied and before a following reset has been applied.

15. The method of claim 14 further comprising reading a value from a resetable storage cell that indicates whether said storage cell has been written to after a reset has been applied.

16. The method of claim 15 wherein said resetable storage cell is a storage cell within a memory having reset capability, said resetable storage cell having the same address as said storage cell.

17. The method of claim 15 wherein said resetable storage cell is a register.

18. A method, comprising:

a) inferring the existence of a resetable memory from a behavioral or RTL level description of a semiconductor circuit; and

b) incorporating a resetable memory design into a design for said semiconductor circuit.

19. The method of claim 18 wherein said incorporating a resetable memory design into a design for said semiconductor circuit further comprises incorporating a gate level resetable memory description into a gate level description of said semiconductor circuit.

20. The method of claim 18 wherein said resetable memory design comprises a memory without reset capability having a data output coupled to a first input of a first multiplexer, a second input of said first multiplexer having a reset value input, a channel select for said first multiplexer coupled to a resetable storage cell output that indicates whether a storage cell within said memory without reset capability has been written to after a reset or has not been written to after a reset.

21. The method of claim 20 wherein said storage cell is a storage cell within a memory unit having reset capability.

22. The method of claim 20 wherein said storage cell is a register.

23. The method of claim 18 wherein said resetable memory design further comprises a memory unit without reset and a rest value write unit that

writes a reset value into storage cells of the memory unit without reset after a reset is applied.

24. The method of claim 18 further comprising inferring a number of clock cycles available for a reset between said inferring the existence and said incorporating.

25. The method of claim 24 wherein said incorporating a resetable memory design further comprises incorporating a resetable memory design having a first memory unit without reset capability and a second memory unit with reset capability if said number of clock cycles corresponds to a first amount of time that is less than a second amount of time in which a reset value can be written into a memory unit without reset capability.

26. The method of claim 24 wherein said incorporating a resetable memory design further comprises a resetable memory design having a reset value write circuit coupled to a memory unit without reset capability if said number of clock cycles corresponds to a first amount of time that is greater than a second amount of time in which a reset value can be written into said memory unit without reset capability.

27. The method of claim 18 wherein said inferring the existence of a resetable memory further comprises identifying within an operational flow of said description that a reset is being applied to a variable.

28. A machine readable medium having stored thereon a sequence of instructions which, when executed by a digital processing system, cause said system to perform a method, said method, comprising:

a) inferring the existence of a resetable memory from a behavioral or RTL level description of a semiconductor circuit; and

b) incorporating a resetable memory design into a design for said semiconductor circuit.

29. The machine readable medium of claim 28 wherein said incorporating a resetable memory design into a design for said semiconductor circuit further comprises incorporating a gate level resetable memory description into a gate level description of said semiconductor circuit.

30. The machine readable medium of claim 28 wherein said resetable memory design comprises a memory without reset capability having a data output coupled to a first input of a first multiplexer, a second input of said first multiplexer having a reset value input, a channel select for said first multiplexer coupled to a resetable storage cell output that indicates whether a storage cell within said memory without reset capability has been written to after a reset or has not been written to after a reset.

31. The machine readable medium of claim 30 wherein said storage cell is a storage cell within a memory unit having reset capability.

32. The machine readable of claim 30 wherein said storage cell is a register.

33. The machine readable medium of claim 28 wherein said resetable memory design further comprises a memory unit without reset and a reset value write unit that writes a reset value into storage cells of said memory unit without reset after a reset is applied.

34. The method of claim 28 further comprising inferring a number of clock cycles available for a reset between said inferring the existence and said incorporating.

35. The method of claim 34 wherein said incorporating a resetable memory design further comprises incorporating a resetable memory design having a first memory unit without reset capability and a second memory unit with reset capability if said number of clock cycles corresponds to a first amount of time that is less than a second amount of time in which a reset value can be written into a memory unit without reset capability.

36. The method of claim 34 wherein said incorporating a resetable memory design further comprises a resetable memory design having a reset value write circuit coupled to a memory unit without reset capability if said number of clock cycles corresponds to a first amount of time that is greater than a second amount of time in which a reset value can be written into said memory unit without reset capability.

37. The method of claim 28 wherein said inferring the existence of a resetable memory further comprises identifying within an operational flow of said description that a reset is being applied to a variable.

38. A resetable memory, comprising:

a memory unit without reset and a reset value write unit that writes a reset value into storage cells of said memory unit without reset after a reset is applied to said resetable memory.